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PTO/SB/05 (12/97)

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. 1.53(b))

Attorney Docket No.	0694/00063
First Named Inventor or Application Identifier	Po-Yao Lin
Title	Integrated Circuit Package with Multiple Heat Dissipation Paths
Express Mail Label No.	

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO: **Assistant Commissioner for Patents**
Box Applications
Washington, DC 20231

1. [X] Filing Fee as calculated below.
2. [X] Specification [Total Pages **[10]**]
(preferred arrangement set forth below)
- Descriptive title of the invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings *(if filed)*
- Detailed Description
- Claim(s)
- Abstract of the Disclosure
3. [X] Drawing(s) *(35 USC 113)* [Total Pages **[2]**]
4. Oath or Declaration [Total Pages **[2]**]
   a. [X] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional with Box 17 completed)*
      [ ] DELETION OF INVENTOR(S)
      Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b)
5. [ ] Incorporation By Reference *(useable if Box 4b is checked)* The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [X] Assignment Papers (cover sheet & document(s))
9. [ ] 37 CFR 3.73(b) Statement [ ] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12. [ ] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
14. [ ] Small Entity Statement(s) [ ] Statement filed in prior application, Status still proper and desired
15. [X] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. [ ] Other:

17. **If a CONTINUING APPLICATION**, *check appropriate box and supply the requisite information:*
☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.

18. CORRESPONDENCE ADDRESS

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Fee Calculation and Transmittal

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	NO. FILED			NO. EXTRA	RATE	FEE		RATE	FEE
TOTAL	12	minus	20	= 0	x9=	$		x18=	$
INDEP	1	minus	3	= 0	x39=	$		x78=	$
___ First Presentation, Multiple Dependent Claims					+130=	$		+260=	$0
Base Filing Fee						$380			$760
Other Fee (specify purpose) Assignment recordal						$			$40
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☒ A check in the amount of $800 to cover the filing fee is enclosed

☐ No payment is enclosed at this time. Full payment will be made when the executed Declaration is submitted.

☒ The Commissioner is hereby authorized to charge and credit Deposit Account No. 22-0185 as described below. A duplicate copy of this sheet is enclosed.

☐ Charge the amount of as filing fee

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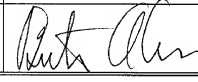
☐ Charge the Issue Fee set in 37 CFR § 1.18 at the mailing of the Notice of Allowance, pursuant to 37 CFR § 1.311(b)

Name (Print/Type)	Burton A. Amernick	Registration No. (Attorney/Agent)	24,852
Signature		Date	Aug. 24, 1999

INTEGRATED CIRCUIT PACKAGE WITH MULTIPLE HEAT DISSIPATION PATHS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an integrated circuit package, and more particularly, to an integrated circuit package with a heat spreader to dissipate heat.

2. Description of Related Art

Because the integrated circuit semiconductor device is getting more complicated in function and smaller in size, the flip chip semiconductor device is seeing more wide-spread use, since flip chip mounting permits a high component density and fast accessing time. FIG. 4 shows a conventional integrated circuit package which is of a well known "flip chip on board" type packaging. By welding the solder bumps 42 of a die 40 to a printed circuit board 41, the die 40 is electrically connected to the printed circuit board 41. An underfill 43 is injected between the die 40 and the printed circuit board 41 to securely consolidate the die 40 with the printed circuit board 41 so that the solder joints between the die 40 and the printed circuit board 41 will not be damaged due to different degrees of thermal expansion of the die 40 and the printed circuit board 41 upon thermal excursions, which the integrated circuit semiconductor device experiences during operation.

However, due to the fact that the aforementioned flip chip semiconductor device is of small volume and with high power density, the thermal resistance greatly increases. The major heat dissipation paths are from the backside of the die 40 to the environment and from the lower portion of the die 40 to the printed circuit board 41. Unfortunately, the underfill filled between the die 40 and the printed

circuit board 41 is of an insulating material, such as epoxy resin, whose heat conducting capability is extremely low. Therefore, the heat from the die 40 is difficult to be conducted to the printed circuit board 41 and the heat dissipation capability of such a flip chip semiconductor device is unsatisfactory.

In order to eliminate the aforementioned heat dissipating problem, an additional heat cap or heat spreader may be employed to assist in dissipating heat. FIG. 5 shows a flip chip integrated circuit package having a die 50 attached to a substrate 53 that is mounted on a printed circuit board 54. A metal heat sink 51 is further mounted on the top of the die 50 via adhesive 52 such that the heat from the die 50 is dissipated to the heat sink 51. With such a flip chip packaging structure, the effective heat dissipating area can be increased by using the heat sink 51. However, the heat sink 51 is secured to the die 50 by adhesive 52, thus the load on the die 50 is heavy so that the connection between the die 50 and the substrate 53 is likely to be damaged due to stress generated by the heavy load. Therefore, the reliability of such a packaged semiconductor device is difficult to promote.

Alternatively, FIG. 6 shows a flip chip integrated circuit package, which has a metal heat cap 61 disposed on a substrate 63 to cover a die 60. The heat cap 61 is adhered to the substrate 63 through epoxy resin 62. A heat conductive adhesive 64 is filled between the heat cap 61 and the die 60. Thus, the heat from the die 60 can be dissipated out through the heat cap 61. With such a packaging structure, the heat cap 61 is adhered to the substrate 63 through the epoxy resin 62 that is unable to transfer heat. Thus, the heat can not be effectively conducted to the substrate 63 to be dissipated. Moreover, the aforementioned heat sink 51 and the heat cap 61 are with large footprints with respect to that of the die 50, 60. However, since the density of the electronic package is

getting higher and the size of electronic product is getting smaller, adding such large heat dissipation elements to the flip chip device is obviously undesired, as it will greatly increase the space required by the flip chip device. Thus, there is a need for the above integrated circuit packages to be improved.

Among the known patents related to the heat dissipation of a flip chip integrated circuit package, U. S. Patent No. 5,847,929 granted to Bernier et al. has disclosed the use of an adhesive of silicone or flexible-epoxy to attach a heat sink to a semiconductor chip. U. S. Patent No. 5,726,079 granted to Johnson has provided a thermally conductive planar member in packaging a flip chip. U. S. Patent No. 5,650,662 granted to Edwards et al. has disclosed a heat spreader that is directly bonded to an electronic device package. U. S. Patent No. 5,856,911 granted to Riley has provided an integrated circuit package having a top die attach area and a bottom heat spreader thermally coupled to the die. The above patents are provided to dissipate heat out of integrated circuit packages with only one heat dissipation path which us from the die upward to the environment. Therefore, they can not be used to effectively solve the aforementioned heat dissipation problems.

SUMMARY OF THE INVENTION

Accordingly, the object of the present invention is to provide an integrated circuit package having a heat spreader to dissipate heat generated by a die both from the backside of the die and by conducting to the printed circuit board, so as to improve the heat dissipating effect. Moreover, the installation of the heat spreader will not increase the load of the die.

To achieve the object, an integrated circuit package is provided which has a printed circuit board and a die attached to the printed

circuit board. A heat spreader secured to the printed circuit board is provided to cover the die and contact with the backside of the die, so that heat from the die can be transferred upward to the environment and downward to the printed circuit board through the heat spreader. Further, since the heat spreader is secured to the printed circuit board, no additional load is added to the die.

The various objects and advantages of the present invention will be more readily understood from the following detailed description when read in conjunction with the appended drawing.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a side cross sectional view of an integrated circuit package in accordance with the present invention;

FIG. 2 is a perspective view showing a heat spreader of the integrated circuit package in accordance with the present invention;

FIG. 3 is a top view of a printed circuit board used in the integrated circuit package in accordance with the present invention;

FIG. 4 is a side cross sectional view of a conventional flip chip integrated circuit package;

FIG. 5 is a side view of a conventional flip chip integrated circuit package with a heat sink; and

FIG. 6 is a side cross sectional view of a conventional flip chip package with a heat cap.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

A preferred embodiment of an integrated circuit package with multiple heat dissipation paths in accordance with the present invention is illustrated in FIG. 1, which has a die 12 attached to a printed circuit board 11. The die 12 has multiple solder bumps 121 at the bottom thereof to mount to the surface of the printed circuit board 11. An underfill 18 is applied between the die 12 and the printed circuit board

11. A heat spreader 13 is provided to cover the die 12. The heat spreader 13 contacts with the backside of the die 12 and is adhered to the printed circuit board 11 for providing additional heat dissipation for the die 12.

With reference to FIG. 2, the heat spreader 13 is preferred to have a shape similar to a lead frame known in the art of integrated circuit packaging. That is, the heat spreader 13 is formed by a rectangular piece body 131 and a plurality of supporting leads 132 extended downward from the periphery of the piece body 131. It is preferable that the heat spreader 13 is made of metal with a high thermal conductivity, such as copper or aluminum.

Referring to FIG. 1 again, the heat spreader 13 of lead frame type is mounted on the printed circuit board 11 in such a manner that the supporting leads 132 thereof stand on the printed circuit board 11, and the piece body 131 substantially abuts on the backside of the die 12. A high thermal conductivity interface, such as thermal grease, is filled between the piece body 131 and the die 12. Therefore, the heat of the die 12 can be conducted upward and thus transferred to the outer environment through the heat spreader 13. Moreover, each supporting lead 132 is spaced from the adjacent one so that a gap 133 is defined between two adjacent supporting leads 132 to allow circuit connection to be directed to the die 13 thereby enabling the transfer of signals to and from the die 12.

With reference to FIG. 3, the surface of the printed circuit board 11 is formed with a plurality of thermal pads 111 disposed around the die 12. At the center of each of the thermal pad 111, a thermal via hole 112 is defined. With reference to FIG. 1 again, the plurality of supporting leads 132 of the heat spreader 13 are secured to the plurality of thermal pads 111 of the printed circuit board 11, respectively,

through solder 15 by surface mounting technology (SMT). Moreover, the printed circuit board 11 has an inner-layered copper plane 16, and the plurality of thermal via holes 112 are connected to the inner-layered copper plane 16. Therefore, other than dissipating heat upwards and out to the environment through the heat spreader 13, the heat from the die 12 can be downwardly conducted to the inner-layered copper plane 16 of the printed circuit board 11 through the plurality of supporting leads 132 and the thermal via holes 112. Accordingly, multiple heat dissipation paths are provided, and an enhanced efficiency of heat dissipation is achieved. Furthermore, the dimension of such an integrated circuit packaging is small so that it can be used in a circuit design requiring a small footprint. Additionally, the aforementioned thermal via holes 112 are not restricted to be defined within the thermal pads 111. It is also applicable to define thermal via holes at positions away from the thermal pads, and such thermal via holes are connected to the corresponding thermal pads by conductive traces plated on the printed circuit board, thereby achieving the same heat dissipation effect.

Other than the enhanced heat dissipation effect, the heat spreader 13 of the integrated circuit package is secured to the printed circuit board 11 by surface mounting technology. Thus, in addition to the known SMT process, no extra process is required to secure the heat spreader 13 to the printed circuit board 11, and the installation of the heat spreader 13 will not become a load to the die 12. Furthermore, since the heat spreader 13 abuts on the die 12 via thermal grease 14 and without adhesiveness, no stress will be applied to the die 12. Therefore, the reliability of the integrated circuit package can be greatly increased.

With reference to FIGs. 1 and 3 again, material with high thermal conductivity, such as conductive adhesive, can be filled between the plurality of supporting leads 132 of the heat spreader 13 and the die 12. The conductive adhesive 17 is condensed in the gaps 133 between the supporting leads 132 by surface tension effect and will not escape out of the heat spreader 13. Thus, the stability of the integrated circuit package and the heat dissipation efficiency can be further enhanced. Besides, an additional heat sink (not shown) can be mounted onto the piece body 131 of the heat spreader 13 to provide extra heat dissipation area, thereby enhancing the heat dissipation effect.

Although the present invention has been described with reference to the preferred embodiments, it will be understood that the invention is not limited to the details described thereof. Various substitutions and modifications have been suggested in the foregoing description, and others will occur to those of ordinary skill in the art. Therefore, all such substitutions and modifications are intended to be embraced within the scope of the invention as defined in the appended claims.

WHAT IS CLAIMED IS:

1. An integrated circuit package comprising:

a printed circuit board;

a die attached to the printed circuit board; and

a heat spreader covering the die, the heat spreader contacting with backside of the die and being mounted to the printed circuit board.

2. The integrated circuit package as claimed in claim 1, wherein the heat spreader is formed by a piece body and a plurality of supporting leads extended downward from a periphery of the piece body.

3. The integrated circuit package as claimed in claim 2, wherein the piece body of the heat spreader abuts on the backside of the die, an interface with high thermal conductivity being filled between the piece body and the die.

4. The integrated circuit package as claimed in claim 3, wherein the interface with high thermal conductivity is thermal grease.

5. The integrated circuit package as claimed in claim 2, wherein the printed circuit board has a surface formed thereon a plurality of thermal pads disposed around the die.

6. The integrated circuit package as claimed in claim 5, wherein the plurality of supporting leads of the heat spreader are secured to the plurality of thermal pads on the printed circuit board, respectively.

7. The integrated circuit package as claimed in claim 6, wherein the plurality of supporting leads are secured to the plurality of thermal pads by surface mounting technology.

8. The integrated circuit package as claimed in claim 5, wherein the printed circuit board defines a plurality of thermal via holes at positions where the plurality of thermal pads are formed, respectively.

9. The integrated circuit package as claimed in claim 5, wherein the printed circuit board has an inner-layered copper plane, the plurality of thermal via holes being connected to the inner-layered copper plane.

10. The integrated circuit package as claimed in claim 5, wherein an additional heat sink is further mounted onto the piece body of the heat spreader.

11. The integrated circuit package as claimed in claim 5, wherein material with high thermal conductivity is filled between the plurality of supporting leads and the die.

12. The integrated circuit package as claimed in claim 1, wherein the material with high conductivity is thermal grease.

ABSTRACT OF THE DISCLOSURE

An integrated circuit package has a printed circuit board, a die mounted on the printed circuit board, and a heat spreader attached to the printed circuit board to cover the die and contact with the backside of the die. The heat spreader is formed by a piece body and a plurality of supporting leads extended downward from the periphery of the piece body. The supporting leads of the heat spreader are attached to the printed circuit board by surface mounting technology. The piece body of the heat spreader abuts on the backside of the die so that heat from the die can be conducted both upward to the outer environment and downward to the printed circuit board through the heat spreader, thereby enhancing the heat dissipation efficiency.

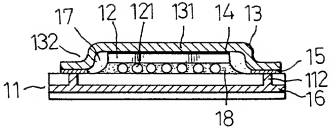


FIG. 1

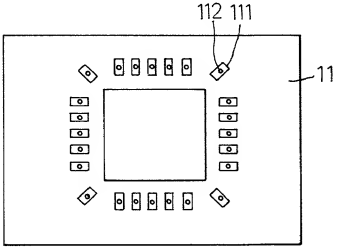


FIG. 3

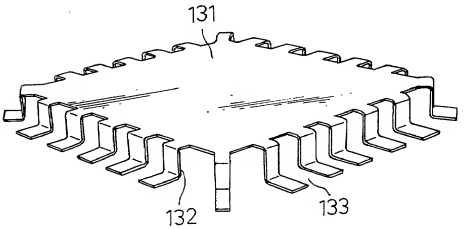


FIG. 2

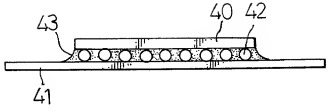


FIG. 4 PRIOR ART

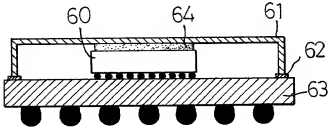


FIG. 6 PRIOR ART

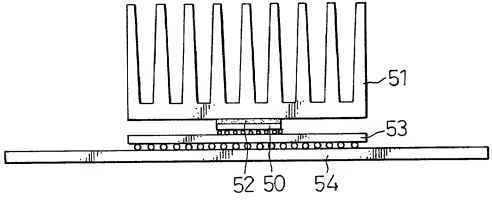


FIG. 5 PRIOR ART

DECLARATION FOR PATENT APPLICATION

As a below-named inventor, I hereby declare that:

My residence, post office and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claim and for which a patent is sought on the invention entitled:

"Integrated Circuit Package With Multiple Heat Dissipation Paths"

the specification of which: (check one)
[X] is attached hereto [ ] was filed on _____, as United States Patent Application Serial No_____ ., or PCT International Application Number _____, and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with 37 CFR § 1.56(a).

Prior Foreign Application(s): I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor certificate listed below, or § 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below any foreign application for patent or inventor certificate having a filing date before that of the application on which priority is claimed:

PRIOR FOREIGN APPLICATION(S)			PRIORITY CLAIMED	
Number	Country	Day/Month/Year Filed	Yes	No
88209607	**Taiwan R.O.C.**	**11/6/1999**	**X**	

I hereby Claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below:

Application No.	Filing Date

I hereby claim the benefit under 35 U.S.C § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by 35 U.S.C. § 112, first paragraph, I acknowledge the duty to disclose material information as defined in 37 CFR § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application Serial No.	U.S. Filing Date	Status – Patented, Pending, Abandoned

I hereby appoint Elliott I. Pollock, Registration No. 16,906; George Vande Sande, Registration No. 17,276; Robert R. Priddy, Registration No. 20,169; Burton A. Amernick, Registration No. 24,852; Stanley B. Green, Registration No. 24,351; Richard Wiener, Registration No. 18,741; Townsend M. Belser, Jr., Registration No. 22,956; Morris Liss, Registration No. 24,510, Martin Abramson, Registration No. 25,787; Geroge R. Pettit, Registration No. 27,369; Elzbieta Chlopecka, Registration No. 32,767; Eric J. Franklin, Registration No. 37,134, and Jeffri A. Kaminski, Registration No. P-42,709, my attorneys with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith.

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(202) 331-7111

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Date 18 Aug. 1999	Signature

[X] See Next Page For additional inventors

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Date 18 Aug. 1999	Signature Hwang, Ching-Bai

Full name of third joint inventor (if any)	Citizenship
Residence Address	Post Office Address [x] Same as Residence
Date	Signature

Full name of forth joint inventor (if any)	Citizenship
Residence Address	Post Office Address [x] Same as Residence
Date	Signature

Full name of fifth joint inventor (if any)	Citizenship
Residence Address	Post Office Address [x] Same as Residence
Date	Signature